UVic Department of Electrical and Computer Engineering

COURSE OUTLINE
CENG 241 – Digital Design
Summer 2014

Instructor:

Dr. Amirali Baniasadi

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Office Hours:

Days: by appointment via 721-8613, or email

Time:
Location: EOW 441

Lectures:

A-Section(s): A01 / CRN 30063
A02 / CRN 30064
Days: Tuesday/Wednesday/Friday
Time: 10:30-11:20
Location: ECS125

Labs: **Location: ELW A359**

B-Section(s): B01 Monday 13:30-16:30
B02 Tuesday 13:00-16:00
B03 Thursday 13:30-16:30
B04 Friday 14:30-17:30
B05 Tuesday 17:00-20:00

Required Text:

Title: **Digital Design, Fitfh Edition**
Author: **M.Morris Mano**
Publisher: **Prentice Hall**
Year:2012

Optional Text:

Title:
Author:
Publisher:
Year:

References:

Assessment:

Assignments:	10%
Labs	30%
Quizzes	30%
Final	30%

Dates: Will be announced in advance

Note: Failure to complete all laboratory requirements will result in a grade of N being awarded for the course.

Due dates for assignments:

The final grade obtained from the above marking scheme will be based on the following percentage-to-grade point conversion:

Passing Grades	Grade Point Value	Percentage For Instructor Use Only	
A+	9	90 - 100	
A	8	85 - 89	
A-	7	80 - 84	
B+	6	77 - 79	
B	5	73 - 76	
B-	4	70 - 72	
C+	3	65 - 69	
C	2	60 - 64	
D	1	50 - 59	
Failing Grades	**Grade Point Value**	**Percentage For Instructor Use Only**	**Notes**
E	0	35 - 49	Fail, conditional supplemental exam.
F	0	0 - 34	Fail, no supplemental exam.
N	0	0 - 49	Did not write examination, Lab or otherwise complete course requirements by the end of the term or session; no supplemental exam.

The rules for supplemental examinations are found on page 80 of the current 2013/14 Undergraduate Calendar.

Term in which E Grade was obtained:	Application Deadline for Supplemental Exam	Supplemental Exam Date
First term of Winter Session (Sept – Dec)	Following February 28	First week of following May
Second term of Winter Session (Jan – Apr)	Following June 30	First week of following September
Summer Session (May – Aug)	Following October 31	First week of following January

Deferred exams will normally be written at the start of the student's next academic term; i.e., approximately 4 months following the deferral of the exam.

Course Description

1. Course Objectives: Understanding, analyzing and designing simple digital systems, including sequential and combinational circuits.
2. Learning Outcomes: Learning to Analyze and Design Digital Circuits
3. Syllabus: Boolean algebra, canonical expressions, logic gates and their physical realization. Fan-in and fan-out, timing, rise and fall times, delay. Combinational circuits minimization (Karnaugh map). Standard circuits - adders, multiplexers, demultiplexers, etc. Memory elements, flip-flops. State transition diagrams, Mealy-Moore finite state machines. State assignment and machine realization, counters. Introduction to Verilog and its use to design combinational and sequential circuits. Advanced topics to include design with PLDs, PLAs, FPGAs.

Guidelines on Religious Observances

See http://web.uvic.ca/calendar2014/GI/GUPo.html

Commitment to Inclusivity and Diversity

The University of Victoria is committed to promoting, providing and protecting a positive, supportive and safe learning and working environment for all its members.

Standards of Professional Behaviour

You are advised to read the Faculty of Engineering document Standards for Professional Behaviour at http://www.engr.uvic.ca/policy/professional-behaviour.php which contains important information regarding conduct in courses, labs, and in the general use of facilities.

Cheating, plagiarism and other forms of academic fraud are taken very seriously by both the University and the Department. You should consult

http://web.uvic.ca/calendar2014/FACS/UnIn/UARe/PoAcI.html for the UVic policy on academic integrity.

Plagiarism detection software may be used to aid the instructor and/or TA's in the review and grading of some or all of the work you submit.