



**Dept. of Electrical and Computer Engineering**  
University of Victoria  
P.O. Box 3055 STN CSC  
Victoria, B.C. V8W 3P6  
CANADA

## **COURSE OUTLINE**

### **CENG 441: Design of Digital and VLSI Systems**

Website: <http://www.ece.uvic.ca/~fayez/courses/ceng441>

**May-August 2014**

#### **Instructor**

Dr. F. Gebali, PhD, PEng  
Phone: 250-721-6509  
E-mail: [fayez@uvic.ca](mailto:fayez@uvic.ca)

#### **Office Hours**

Days: Everyday  
Time: Drop in or phone first  
Location: EOW 451

#### **Lectures**

Days: Mon & Thu  
Time: 10:00 – 11:20  
Location: CLE A307

#### **Labs**

Check Course Webpage

#### **Textbook**

Lecture notes by Dr. Gebali available on course web page

#### **Assessment**

<b>Activity</b>	<b>Grade</b>
Preliminary Design Presentation	10 %
Midterm Progress Report	10 %
Final Presentation	20 %
Final Project Demo	30 %
Final Report	30 %
<b>Total</b>	<b>100%</b>

#### **CENG 441 Percentage-To-Grade Point Conversion:**

The final grade obtained from the above marking scheme will be based on the following table:

<b>Passing</b>	<b>Grade Point Value</b>	<b>Percentage</b>
A+	90-100	
A	85-89	
A-	80-84	
B+	77-79	
B	73-76	
B-	70-72	
C+	65-69	
C	60-64	
D	50-59	
E	35-49	Fail, conditional supplemental exam.
F	0 -35	Fail, no supplemental exam.
N		Fail, did not write examination, lab or otherwise complete course requirements by the end of the term or session; no supplemental exam.

## Course Description

1. **Course Objectives:** Study digital system and VLSI design methodology, design for testability and design verification. Learn methods to improve digital VLSI systems performance: reliability, manufacturability, cost, power, security, etc. Learn hardware design language (HDL) and assertion-based verification language (ABVL).
2. **Learning Outcomes:** The learning outcomes of this course enable students to:
  - (a) Design design complex digital systems using VLSI design methodology.
  - (b) Design a digital system using given specifications and design constraints.
  - (c) Assess logic and technology-specific parameters to control the functionality, system synchronization, power consumption, and effects of circuit parasitics.
  - (d) Plan and choose digital system testing strategy
  - (e) Plan digital system verification strategy
  - (f) Design a significant VLSI design project having a set of objective criteria and design constraints.
3. **Syllabus:**
  - (a) VLSI overview
  - (b) VHDL overview
  - (c) VLSI design methodology
  - (d) VLSI design options
  - (e) VHDL language basics
  - (f) VHDL combinational logic modeling
  - (g) VHDL sequential logic modeling
  - (h) VHDL RTL synthesis basics
  - (i) Overview of hardware verification
  - (j) Assertion-based verification (ABV)
  - (k) Design for test (DFT)

## Guidelines on Religious Observances

1. Where classes or examinations are scheduled on the holy days of a religion, students may notify their instructors, at least two weeks in advance, of their intention to observe the holy day(s) by absenting themselves from classes or examinations.
2. Instructors will provide reasonable opportunities for such students to make up work or missed examinations.
3. Students will cooperate by accepting the provision of reasonable opportunities for making up work or missed examinations.
4. The University Secretary's Office will distribute a multi-faith calendar to each academic unit annually.

## Commitment to Inclusivity and Diversity

The University of Victoria is committed to promoting, providing and protecting a positive, supportive and safe learning and working environment for all its members.

## Standards of Professional Behaviour

You are advised to read the Faculty of Engineering document Standards for Professional Behaviour at <http://www.engr.uvic.ca/policy/professional-behaviour.php> which contains important information regarding conduct in courses, labs, and in the general use of facilities.

Cheating, plagiarism and other forms of academic fraud are taken very seriously by both the University and the Department. You should consult <http://web.uvic.ca/calendar2010/FACS/UnIn/UARe/PoAcI.html> for the UVic policy on academic integrity.