University of Victoria Engineering

Faculty of Engineering

COURSE OUTLINE

CENG 241 – Digital Design

Term – SUMMER 2015 (201505)

Instructor

Dr. Amirali Baniasadi
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Office Hours

Days: by appointment via 721-8613, or email

Location: EOW 441

Course Objectives

Understanding, analyzing and designing simple digital systems, including sequential and combinational circuits.

Learning Outcomes

- Learning to Analyze and Design Digital Circuits

Syllabus

-Boolean algebra, canonical expressions, logic gates and their physical realization. Fan-in and fan-out, timing, rise and fall times, delay. Combinational circuits minimization (Karnaugh map). Standard circuits - adders, multiplexers, demultiplexers, etc. Memory elements, flip-flops. State transition diagrams, Mealy-Moore finite state machines. State assignment and machine realization, counters. Introduction to Verilog and its use to design combinational and sequential circuits. Advanced topics to include design with PLDs, PLAs, FPGAs

Lectures

A-Section(s): A01 / CRN 30084 A02/30085
Days: Tue, Wed, Fri
Time: 1030 - 1120
Location: ECS 125

Labs: **Location: ELW A359**

B01	Mon 8:30-11:30	Saman (samankh@uvic.ca)
B02	Tue 13:00-16:00	Alex (adimopou@uvic.ca)
B03	Mon 13:30-16:30	Sabuj (sdgupta@uvic.ca)
B04	Thu 8:30-11:30	Ali (jooya@uvic.ca)
B05	Thu 13:30-16:30	Chamira (chamira@uvic.ca)

Required Text

Title: **Digital Design, Fifth Edition**
Author: **M. Morris Mano**
Publisher: **Prentice Hall**
Year: 2012

Optional Text

Title:
Author:
Publisher:
Year:

References:

Assessment:

Assignments:	10%	Due Dates:
Labs	30%	
Quizzes	30%	Date:
Final Exam	30%	

Note: **(sample notes for the instructors)**
Failure to complete all laboratory requirements will result in a grade of N being awarded for the course.
Failure to pass the final exam will result in a failing grade for the course.

The final grade obtained from the above marking scheme for the purpose of GPA calculation will be based on the percentage-to-grade point conversion table as listed in the current Undergraduate Calendar.

There will be no supplemental examination for this course.

(OR)

Assignment of E grade and supplemental examination for this course will be at the discretion of the Course Instructor. The rules for supplemental examinations can be found in the current Undergraduate Calendar.

http://web.uvic.ca/calendar/FACS/UnIn/UARe/Grad.html

Note to Students:

Students who have issues with the conduct of the course should discuss them with the instructor first. If these discussions do not resolve the issue, then students should feel free to contact the Chair of the Department by email or the Chair's Secretary to set up an appointment.

Accommodation of Religious Observance
http://web.uvic.ca/calendar/GI/GUPo.html

Policy on Inclusivity and Diversity
http://web.uvic.ca/calendar/GI/GUPo.html

Standards of Professional Behaviour

You are advised to read the Faculty of Engineering document Standards for Professional Behaviour in current Undergraduate Calendar, which contains important information regarding conduct in courses, labs, and in the general use of facilities.

Cheating, plagiarism and other forms of academic fraud are taken very seriously by both the University and the Department. You should consult entry in current Undergraduate Calendar for the UVic policy on academic integrity.

http://www.uvic.ca/engineering/assets/docs/professional-behaviour.pdf

Course Lecture Notes

Unless otherwise noted, all course materials supplied to students in this course have been prepared by the instructor and are intended for use in this course only. These materials are NOT to be re-circulated digitally, whether by email or by uploading or copying to websites, or to others not enrolled in this course. Violation of this policy may in some cases constitute a breach of academic integrity as defined in the UVic Calendar.