CENG 441 – Design of Digital and VLSI Systems

May-Aug 2015 (30100, 30101)

Instructor
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Office Hours
Days: Everyday
Time: Drop in but phone first
Location: EOW 451

Lectures
Days: Mon, Thu
Time: 10:00 – 11:20
Location: HHB 110

Labs
Check Course Webpage

Course Objectives

Study complex digital system design and VLSI design methodology. Learn methods to improve digital VLSI systems performance: delay, speed, power, area. Learn hardware design language for design entry. Learn design for test techniques.

Learning Outcomes

Upon completion of this course you will acquire the following skills:

1. Design complex digital systems using VLSI design methodology.

2. Develop system specifications.

3. Develop digital systems using given specifications.

4. Assess logic and technology-specific parameters to control the functionality, system synchronization, power consumption, and effects of circuit parasitics.

5. Plan digital system testing strategy

6. Plan digital system verification strategy

7. Design a significant VLSI design project having a set of objective criteria and design constraints.

Syllabus

1. VLSI overview
2. VHDL overview
3. VLSI design methodology
4. VLSI design options
5. VHDL language basics
6. VHDL combinational logic modelling
7. VHDL sequential logic modelling
8. VHDL RTL synthesis basics
9. Design for test (DFT)
10. Digital System Verification

Required Text

Lecture notes by Dr. Gebali.

Assessment

Activity	Grade
Initial Design & Presentation	10 %
Progress Report	10 %
Final Presentation	20 %
Project Functionality Demo	30 %
Final Report	30 %
Total	100 %

The final grade obtained from the above marking scheme for the purpose of GPA calculation will be based on the percentage-to-grade point conversion table as listed in the current Undergraduate Calendar.

There will be no supplemental examination for this course.

`http://web.uvic.ca/calendar/FACS/UnIn/UARe/Grad.html`

Note to Students

Students who have issues with the conduct of the course should discuss them with the instructor first. If these discussions do not resolve the issue, then students should feel free to contact the Chair of the Department by email or the Chair's Secretary to set up an appointment.

Accommodation of Religious Observance

`http://web.uvic.ca/calendar/GI/GUPo.html`

Policy on Inclusivity and Diversity

`http://web.uvic.ca/calendar/GI/GUPo.html`

Standards of Professional Behaviour

You are advised to read the Faculty of Engineering document Standards for Professional Behaviour in current Undergraduate Calendar, which contains important information regarding conduct in courses, labs, and in the general use of facilities.

Cheating, plagiarism and other forms of academic fraud are taken very seriously by both the University and the Department. You should consult entry in current Undergraduate Calendar for the UVic policy on academic integrity.

`http://www.uvic.ca/engineering/assets/docs/professional-behaviour.pdf`

Course Lecture Notes

Unless otherwise noted, all course materials supplied to students in this course have been prepared by the instructor and are intended for use in this course only. These materials are NOT to be re-circulated digitally, whether by email or by uploading or copying to websites, or to others not enrolled in this course. Violation of this policy may in some cases constitute a breach of academic integrity as defined in the UVic Calendar.